REMARKS

Claims 1-14, 36 and 37 are pending in this application. By this Amendment, claims 2, 9, 11, 12 and 37 have been amended. The applicant respectfully submits that no new matter as been added. It is believed that this Response is fully responsive to the Office Action dated July 31, 2001.

Allowable Subject Matter:

Applicant gratefully acknowledges the Examiner's indication that independent claims 1, 4 and 36 are allowable. (See page 5 of the outstanding Action).

Rejection Under 35 U.S.C. §112, First Paragraph:

Claims 9-11, 13 and 37 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, has possession of the claimed invention.

This rejection is respectfully traversed.

However, according to the amendments of claims 9, 11 and 37 as described above, it may be clear that the end of the contact hole is defined by the first and the second sidewall insulation film, and the width of the contact hole is defined by the first and the second sidewall insulation film.

Additionally, it would be common sense that widths of each of the sidewall insulation films are substantially the same width, because the sidewall insulation films are simultaneously formed under the same conditions.

Thus, it is believed that the claimed invention is disclosed, e.g., Fig. 1 of the present application. It is also believed that any scales or specific dimensions are not required for characterizing the above features of the present invention.

Accordingly, withdrawal of the rejection of claims 9-11, 13 and 37 under 35 U.S.C. §112, first paragraph, is respectfully solicited.

Rejection Under 35 U.S.C. §112, Second Paragraph:

Claims 2, 3, 5-8, 12 and 14 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

This rejection is respectfully traversed.

The Examiner states that the specification and drawings disclose that the first insulation film is not present between the two adjacent conductor patterns because of the contact hole. However, it is apparent from amended claims 2 and 12 that the contact hole is located in a par of a region

between the adjacent contact patterns (or the bit lines). As shown in , e.g., Figs. 8A, 9D-9E and 13B, the contact hole 70 is located in a part of a region between the adjacent conductor patterns 56. The first insulation film 64 is filling spaces between the two adjacent conductor patterns 56 where the contact hole 70 is not formed.

The Examiner also states that the specification and drawings disclose that the first insulation film does extend over the etching stopper film. It extends above the film and beyond the etching stopper film where the contact hole is not present. However, as shown in e.g., Figs. 8A and 9D-9E, the first insulation film 64 does not extend over the etching stopper film 58.

Accordingly, withdrawal of the rejection of claims 2, 3, 5-8, 12 and 14 under 35 U.S.C. §112, second paragraph, is respectfully solicited.

As To The Merits:

As to the merits of this case, the Examiner sets forth the following rejections:

(1) claims 2, 3, and 5-8 stand rejected under 35 U.S.C. §102(b) based on **Hiroshi** (JP 08-037181(A); and

(2) claims 9-14 and 37 stand rejected under 35 U.S.C. §103(a) based on **Hiroshi**.

Both of these rejections are respectfully traversed.

Claims 2, 12 and their dependent claims have one feature that the insulation film fills the spaces between the two conductor patterns where the contact hole is not formed and does not extend over the etching stopper film. Based on this feature, according to the present invention, micronized contact holes can be formed without forming the micronized photoresist pattern (see, e.g., page 37, line 9 through page 38, line 8 of the specification of the present application) and the depth of the contact hole can be shallow.

Additionally, according to the claimed invention, the width of the contact hole is determined by the space between the two conductor patterns, so that the stable contact area can be obtained. Thus, the stable and lowered contact resistance can be obtained.

However, in **Hiroshi**, the insulation film 2 extends over the etching stopper film 6 (se, e.g., Fig. 1 of **Hiroshi**), and the width of the contact hole 9 is not determined by the space between the two conductor patterns 5. Thus, above described effects obtained by the present invention are not achieved by **Hiroshi**. **Hiroshi** neither teaches nor suggests that the insulation film is not extending over the etching stopper film and the width of the contact hole is determined by the space between the two conductor patterns.

Thus, **Hiroshi** is clearly different from the claimed invention and does not provide any

motivation for the present invention.

Claims 9, 11, 37 and their dependent claims have one feature that the contact hole has a first width which is larger than a space between the two conductor patterns, and a second width which is substantially the same as a width subtracted twice a width of the second sidewall insulation film from the space between the two conductor patterns. Based on the feature, the present invention can provide the useful effect that the side of the contact hole does not change even when disalignment takes place in the lithography step for opening the contact hole (see the First Embodiment of the present application).

On the other hand, in **Hiroshi**, a width at a top of the contact hole 9 is smaller than a space between the two conductor patterns 5. A width at a bottom of the contact hole 9 is smaller than a width subtracted twice a width of the sidewall insulation film 10, 11 or 12 from the space between the two conductor patterns 5 (see, e.g., Fig. 1 of **Hiroshi**). The above-described effect can not be achieved by the constitution of **Hiroshi**.

Additionally, in **Hiroshi**, as shown in Fig. 1, the structure between the gate electrode 5 on the left side of Fig. 1 and the contact hole 9, and the structure between the gate electrode 5 on the right side of Fig. 1 and the contact hole 9 are not symmetrical. Thus, the coupling capacitances between the gate electrodes 5 and the contact electrode buried in the contact hole 9 are not the same. On the other hand, according to the present invention, the coupling capacitances between the word

lines and the contact electrodes buried in the contact holes can be substantially the same. Whereby the operational margin of the circuit can be improved.

The Examiner states that although **Hiroshi** shows that the sidewall insulation film is formed only one of the gate structures, one of ordinary skill in the art can form the same structure on another gate structure if needed. However, the necessity of such a structure cannot be perceived without perceiving the above described effects. **Hiroshi** neither teaches nor suggests the above described structure and effects.

Thus, **Hiroshi** is clearly different from the claimed invention and does not provide any motivation for the present invention.

In view of the aforementioned amendments and accompanying remarks, claims 1-14, 36 and 37, as amended, are in condition for allowance, which action, at an early date, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated

below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON, LLP

Thomas E. Brown
Attorney for Applicant
Reg. No. 44,450

Atty. Docket No. 980446
1725 K Street, N.W., Suite 1000
Washington, D.C. 20006
Tel: (202) 659-2930
TEB/kas
Enclosures: Version With Markings To Show Changes Made
H:\FLOATERS\TEB\teb\98\980446\Amend 1.111.frm

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 2, 9, 11, 12 and 37 have been amended as follows:

2. (Four Times Amended) A semiconductor device comprising:

a base substrate;

a first conducting film formed over the base substrate and including a plurality of conductor patterns adjacent to each other;

an etching stopper film covering an upper surface of the conductor patterns;

a contact hole located in a part of a region between the adjacent conductor patterns and having an end thereof defined by the conductor patterns;

a first insulation film which is filling spaces between said plurality of conductor patterns where the contact hole is not formed and not extending over the etching stopper film; and

a sidewall insulation film formed on an inner wall of the contact hole so that side walls of the conductor pattern and the etching stopper film are covered.

9. (Four Times Amended) A semiconductor device comprising:

a semiconductor substrate;

a plurality of word lines formed over the semiconductor substrate and extended in a first

direction;

an etching stopper film covering upper surfaces of the word lines;

a first insulation film formed over the etching stopper film and the semiconductor substrate;

[a contact hole] an opening, located between the word lines, reaching the semiconductor substrate through the first insulation film; [and]

a first sidewall insulation film, formed in the [contact hole] opening, covering a side wall of the first insulation film[,];

a second sidewall insulation film, formed in the opening, covering side walls of a stacked layer of the word lines and [side walls of] the etching stopper film[,]; and

a contact hole formed in the opening, reaching the semiconductor substrate, the first sidewall insulation film and the second sidewall insulation film defining an end of the contact hole, the contact hole having a first width ends of which are defined by the first sidewall insulation film and a second width ends of which are defined by the second sidewall insulation film,

[the contact hole having a] the first width [which is] being larger than a space between the adjacent word lines [at a top of the contact hole] and [a] the second width [which is] being substantially the same as a width subtracted twice a width of the second sidewall insulation film from the space between the adjacent word lines [at a bottom of the contact hole].

11. (Four Times Amended) A semiconductor device comprising:

a semiconductor substrate;

a plurality of word lines formed over the semiconductor substrate and extended in a first direction;

a first insulation film formed over the word lines and the semiconductor substrate;

a plurality of bit lines formed over the first insulation film and extended in a second direction;

an etching stopper film covering upper surfaces of the bit lines;

a second insulation film formed over the etching stopper film and the first insulation film;

[a contact hole] an opening, located between the adjacent bit lines;

a first sidewall insulation film, formed in the [contact hole] opening, covering a side wall of the second insulation film[,];

a second sidewall insulation film, formed in the opening, covering side walls of a stacked layer of the bit lines and [side walls of] the etching stopper film[,];

a contact hole formed in the opening, reaching the semiconductor substrate, the first sidewall insulation film and the second sidewall insulation film defining an end of the contact hole, the contact hole having a first width ends of which are defined by the first sidewall insulation film and a second width ends of which are defined by the second sidewall insulation film; and

a capacitor having one electrode connected to the semiconductor substrate through the contact hole,

[the contact hole having a] the first width [which is] being larger than a space between the adjacent bit lines [at a top of the contact hole] and [a] the second width [which is] being substantially the same as a width [substrate] subtracted twice a width of the second sidewall insulation film from the space between the adjacent bit lines [at a bottom of the contact hole].

12. (Four Times Amended) A semiconductor device comprising:

a semiconductor substrate;

a plurality of word lines formed over the semiconductor substrate and extended in a first direction;

a first insulation film formed over the word lines and the semiconductor substrate;

a plurality of bit lines formed over the first insulation film and extended in a second direction;

an etching stopper film covering upper surfaces of the bit lines;

a contact hole located in a part of a region between the adjacent bit lines, having ends thereof defined by the bit lines;

a second insulation film which is filling spaces between said plurality of bit lines where the contact hole is not formed and not extending over the etching stopper film;

a sidewall insulation film, formed in the contact hole, covering a side wall of the second insulation film, side walls of the bit lines and side walls of the etching stopper film; and

a capacitor having one electrode connected to the semiconductor substrate through the contact hole.

37. (Twice Amended) A semiconductor device comprising:

a base substrate;

a first conducting film formed over the base substrate and including two conductor patterns adjacent to each other;

an etching stopper film covering each upper surface of the two conductor patterns;

a first insulation film formed over the etching stopper film and the base substrate;

[a contact hole] an opening, located between the two conductor patterns, reaching the base substrate through the first insulation film; [and]

a first sidewall insulation film, formed in the opening covering [on an inner] a side wall of the first insulation film[,] ;

a second sidewall insulation film, formed in the opening covering an each side wall of a stacked layer of the two conductor patterns[,] and [each side wall of] the etching stopper film [in the contact hole,] ; and

a contact hole formed in the opening, reaching the base substrate, the first sidewall insulation film and the second sidewall insulation film defining an end of the contact hole, the contact hole having a first width ends of which are defined by the second sidewall insulation film

and a second width ends of which are defined by the first sidewall insulation film,

[the contact hole having a] the first width [which is] being larger than a space between the two conductor patterns [at a top of the contact hole] and [a] the second width [which is] being substantially the same as a width subtracted twice a width of the sidewall insulation film from the space between the two conductor patterns [at a bottom of the contact hole].